ABSTRACT

Systems, methods, software products utilize fast analysis information during detailed analysis of a circuit design. One or more design blocks of the circuit design are electronically analyzed to determine fast analysis results based upon assumptions of ported signal nets of each one of the design blocks. Next, it is determined whether hierarchical signal net connectivity of block instances of the design blocks and the assumptions match. If the hierarchical signal net connectivity matches the assumptions, the fast analysis results are utilized to generate detailed analysis results. If the hierarchical signal net connectivity does not match the assumptions, the one or more blocks in the hierarchical signal net connection are electronically analyzed to generate detailed analysis results.